Serial Number: 09/893,023 Filing Date: June 27, 2001

Title: LOW LOSS INTERCONNECT STRUCTURE FOR USE IN MICROELECTRONIC CIRCUITS

Assignee: Intel Corporation

REMARKS

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This responds to the Office Action mailed on June 29, 2004.

Claims 30, 40, 42, 44, and 45 are amended, no claims are canceled, and no claims are added; as a result, claims 13-18 and 26-47 are now pending in this application. The amendments to the claims are fully supported by the specification as originally filed. No new matter is introduced. The amendments are made to clarify the claims and are not intended to limit the scope of equivalents to which any claim element may be entitled. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments above and the remarks that follow.

Claims 30, 40, 42, 44, and 45 are amended to correct a typographical error and not due to prior art.

§103 Rejection of the Claims

Claims 27, 28 and 31-33 were rejected under 35 USC § 103(a) as being unpatentable over Lee et al. (U.S. 6,144,224) in view of Chi (IEEE Transactions on Computers, Vol. 43, No. 5, May 1994)/ Chi (U.S. 5,387,885). Applicant respectfully traverses these grounds of rejection of these claims.

Applicant cannot find a teaching or suggestion in the combination of Lee et al. (hereafter Lee) and Chi (IEEE Transactions on Computers, Vol. 43, No. 5, May 1994)/ Chi (U.S. 5,387,885) of a microelectronic die including a first and second differential signal lines on a first metal layer of the microelectronic die to carry a differential version of a clock signal, where the first and second differential signal lines are substantially parallel to one another, as recited in claim 27. Lee deals with a clock distribution network for a VLSI circuit where "[a]ccording to the invention, two wires emanating from the clock in opposite directions are used to route clock signals from the clock source to the tapping point near the circuit component." See Lee Summary. Two lines emanating from a clock in opposite directions for a VLSI circuit does not teach or disclose two parallel differential lines configured to carry a differential clock signal on a microelectronic die as recited in claim 27. For instance, 44a and 44b referenced in the Office Action carry clock signals in opposite directions. See, Lee, column 5, lines 37-42. Lee lacks a teaching or suggestion regarding differential clock signals on differential signal lines.

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Neither of the Chi documents cures the abovementioned deficiency in applying Lee with respect to claim 27. Chi (U.S. 5,387,885) mentions in Chi's claim 18 an electromagnetic wave propagating on conducting layers in a three dimensional space in a multilayered printed circuit board, where the electromagnetic wave is received in differential signal mode. However, Applicant cannot find in the Chi patent further details regarding the multilayered printed circuit board to receive an electromagnetic wave in differential signal mode nor a teaching regarding differential signal lines to carry a differential clock on a microelectronic die as recited in claim 27.

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Since neither the Lee nor the Chi documents teaches or suggests differential signal lines to carry a differential version of a clock signal on a microelectronic die as recited in claim 27, the combination of Lee and Chi fails to teach all the elements as recited in claim 27. Thus, Applicant submits that at least for the above reasons, claim 27 is patentable over Lee in view of Chi (IEEE Transactions on Computers, Vol. 43, No. 5, May 1994)/ Chi (U.S. 5,387,885).

Claims 28 and 31-33 depend on claim 27 and are patentable over Lee in view of Chi (IEEE Transactions on Computers, Vol. 43, No. 5, May 1994)/ Chi (U.S. 5,387,885) for at least the reasons stated above with respect to claim 27 and further in view of the elements of these dependent claims.

Applicant respectively requests withdrawal of these rejections of claim 27, 28, and 31-33, and reconsideration and allowance of these claims

Allowable Subject Matter

Claims 13-18, 26, 29, 30 and 34-47 were allowed.

Applicant acknowledges allowance of claims 13-18, 26, 29, 30, and 34-47.

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Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2157) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date 10 Seffenber 2004

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this Odd day of September, 2004.

FACIA LEE

Signature

Name